REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the Office Action dated 10 February 2006. Responsive to the rejections made by the Examiner in the Office Action, Independent Claim 1 and Claims 2-12 of the Specification have been amended.

In the Office Action, the Examiner objected to the Specification due to numerous grammatical errors. Accordingly, the Specification has been amended and a Substitute Specification has been appended to this Amendment. It is believed that the amendments to the specification are purely formal in nature and thus no new matter has been added.

Additionally, the Examiner objected to Claim 5 due to grammatical errors. Accordingly, Claim 5 has been corrected.

Finally, the Examiner rejected Claims 1-12 under 35 U.S.C. § 103(a) as being unpatentable over Merkin et al. (Patent # 5,634,137) in view of Delp et al. (Patent # 6,601,200). In setting forth this rejection, the Examiner acknowledged that Merkin et al. fails to disclose a configuration test process, but cited Delp et al. for disclosing as much.

Prior to discussing the prior art relied upon, it is believed beneficial to first briefly describe the Applicant's invention in light of the pending Claims, the Specification and the Drawings. The Claims now more clearly recite the unique

method, which provides many advantages over the prior art. Among the features of the inventive method for testing the pre-designated configuration space settings of a chip are: providing a main board that includes a chip to be tested and a basic input/output system (BIOS) program, which includes a configuration test process for testing the configuration space settings of a chip. Such configuration space settings are those of the type formed in a portion of memory space that is addressable in a chip (In many applications, a certain part of this configuration space is standardized while the remaining part is available for user-defined purposes). When power is started for the main board, in accordance with the claimed method, a power-on self-test (POST) is performed. After the POST has been executed, the BIOS program is loaded and subsequently the pre-designated configuration space on the chip is tested for proper settings.

Merkin et al. discloses a data processing system that tests the system configuration as well as redefines the configuration automatically when any irregularity is detected as a result of a change of hardware.

It is respectfully submitted that the Merkin et al. reference fails among other things to show "... a BIOS program including a configuration space setting test process therein", as defined in amended Independent Claim 1. In fact, it has been noted by the Examiner, that Merkin et al does not show a configuration test process at all. Merkin, et al. discloses at best a particular POST routine, which responds to a change in a hardware system modification. The POST routine of

Merkin, et al does not include a configuration test process, rather it is merely re-executed according to a re-defining of the system, Col 4 lines 43-56. Nowhere does Merkin et al even suggest the testing of a chip's configuration space, much less in the manner now more clearly recited by newly-amended Independent Claim 1.

Thus, as Merkin et al. fails to disclose each and every element of the invention of the subject Patent Application, as now claimed, it hardly anticipates the invention. Further, as the reference fails to suggest such a unique method and in fact fails to recognize the problem solved by the claimed invention, it does not make obvious the invention of the subject Patent Application.

The Delp et al. reference does not overcome the deficiencies of Merkin et al. Delp et al. discloses an integrated circuit including a control and monitor interface that includes on-chip support for one or more network protocols. The Examiner equated the test process of Delp, et al., as shown in column 1, lines 36-44, column 7, lines 55-67 and column 8, line 56 through column 9, line 8 to the configuration space test process of the subject Patent Application. Among other things, however, the configuration process as shown in columns 7-9 is directed to a computer system and a control and monitor mechanism that includes on-chip support and defines various operations to be performed on the chip. Delp et al's test process is not actually directed to the testing of a given chip's configuration space per se. Nor is it one that executes through "...a BIOS program including a

configuration space setting test process therein", as defined in amended Independent Claim 1. Delp et al. clearly teaches away from such features now more clearly recited by the pending claims.

It is respectfully submitted that neither Merkin et al. nor Delp et al. discloses the unique combinations of steps now more clearly recited in the pending claims for the purposes and objectives disclosed in the subject Patent Application

Therefore, it is believed that Independent Claim 1 recites a method that is novel and non-obvious over the cited references and consequently believed to be in condition for allowance. That being so, it is also believed that dependent Claims 2-12 are allowable for at least the same reasons for which the Claim on which they are based is allowable.

The remaining references cited by the Examiner but not used in the rejection have been reviewed and are believed to be even further removed from the Applicant's claimed method when patentability considerations are taken properly into account.

In view of the foregoing amendments and remarks, Applicant believes that the subject Patent Application is now in condition for allowance and such action is respectfully requested.

Respectfully submitted,
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